DESIGN AND PERFORMANCE OF A 2-18 GHz MONOLITHIC MATRIX AMPLIFIER

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Abstract: The paper discusses the design and the performance of the first monolithic matrix amplifier. A gain of 15.5 $\pm$ 0.9 dB at a worst return loss of -12 dB, a maximum noise figure of 7 dB, and a minimum output power of $P_{1\,dB}$ = 15.5 dBm were obtained in the two-tier module across the 2-18 GHz frequency band.

I. INTRODUCTION

The concept of the matrix amplifier integrates the principles of additive and multiplicative amplification in one and the same module [1] and [2]. The resulting circuit, whose schematic is shown in Figure 1, forms a network in which the active devices are positioned in a rectangular array, very much like the mathematical elements in a matrix. The amplifier that is the subject of this paper utilizes eight MESFETs evenly distributed over two tiers. Its gain, noise figure, VSWR, and output power performance are subject of the following discussion. In addition, a brief description of the circuit design and its fabrication will be presented. The unit's environmental behavior over the temperature range of -55°C to +95°C will also be described.

II. CIRCUIT DESIGN AND FABRICATION

The schematic of the 2 x 4 matrix amplifier is shown in Figure 1, while Figure 2 presents a photograph of the 1.9 x 2.3 mm chip. The latter reflects the layout and the line dimensions. A total of four identical MESFETs are located in each of two tiers and are linked horizontally as well as vertically by transmission-line elements. Except for the gate line, each idle port is terminated into an impedance consisting of a resistor shunted by a shorted transmission line. This technique allows biasing of the active

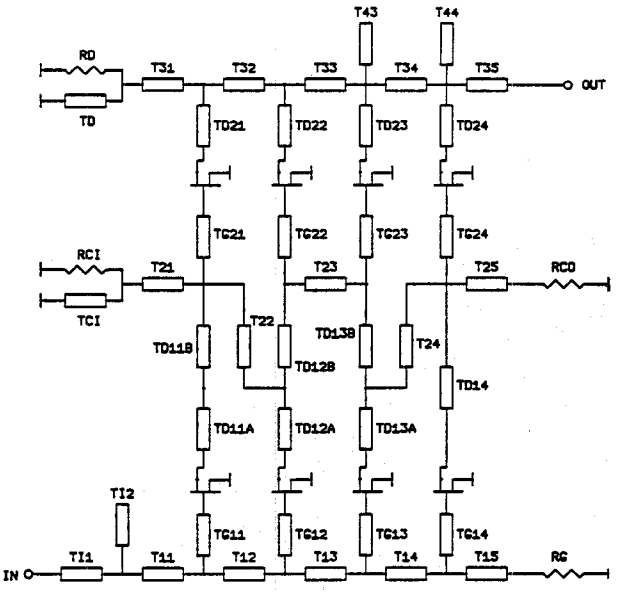

Figure 1 Schematic of the Matrix Amplifier

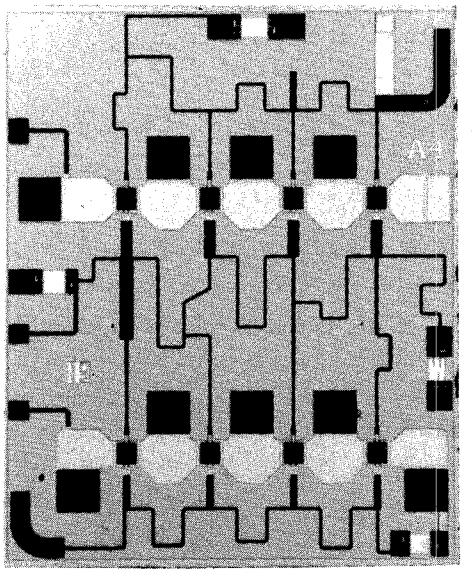

Figure 2 Photograph of the Monolithic Amplifier Chip

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devices without any power dissipation in the termination resistors. The choice of the termination elements is critical for gain flatness and gain slope, as well as stability. The sources of all MESFETs are coupled to ground through thin-film capacitors and via holes which are clearly visible in the photograph of Figure 3. The via holes centered on 175 x 175 μm pads are laser drilled and measure 55-60 μm in diameter. The active devices are fabricated on MBE material with a doping concentration of 4.4 x 17^{17} cm^{-3}. Their gate dimensions are 0.35 x 200 μm. Some of the MESFETs' vital statistics are g_m = 42 mS, C_{gs} = 170 fF, C_{gd} = 14 fF, C_{ds} = 35 fF, and R_{ds} = 280 Ω. The terminations are thin-film resistors using TiWN as resistive material. The MIM capacitors have a capacitance of 0.6 fF/μm^2 and are used either as dc blocks or rf-bypass capacitors. Their breakdown voltage is between 30 volts and 40 volts.

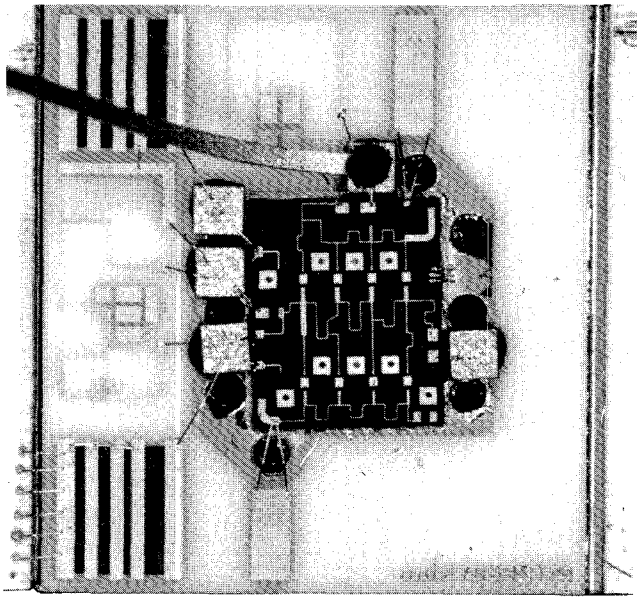

Figure 3 Photograph of the Amplifier Module

As can be seen in the photograph of Figure 3, the chip is mounted on a 5.3 x 5.8 x 0.38 mm alumina substrate, which contains part of the biasing circuitry, including the source-bias resistors, as well as the 50 Ω input and output lines. Separating the biasing network from the monolithic chip and fabricating it on the alumina substrate serves two purposes. First, it provides for an option to moderately tune the circuit and, therewith, improve the amplifier's gain flatness and reflection losses. Second, it significantly reduces the overall chip size and, consequently, the chip costs. Especially, the first function may become a decisive factor in the success or the failure of meeting the required performance specifications which, of course, depend heavily on the uniformity and repeatability of the transistor parameters. The amplifier is energized by a single dc voltage in accordance with the schematic of Figure 4 such that the same dc current passes through both tiers.

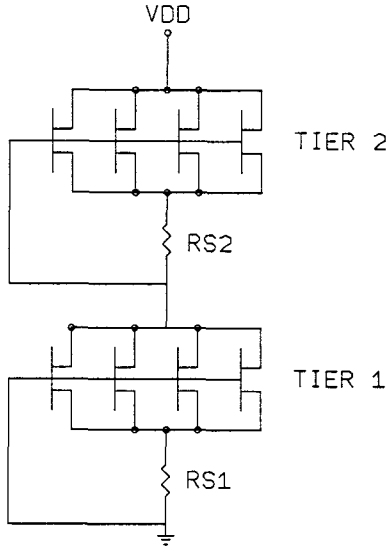

Figure 4 Biasing Scheme of the Amplifier

III. EXPERIMENTAL RESULTS

The test results of the experimental monolithic matrix amplifier, as shown in Figure 3, are plotted in Figure 5. The unit's supply voltage and current in our tests were V_{BIAS} = 9.0 V and I_{BIAS} = 108 mA, respectively. A small-signal gain of 15.5 $\pm$ 0.9 dB and a maximum noise figure of 7 dB were recorded over the 2-18 GHz bandwidth. The maximum return loss is -12.5 dB for the input and -12 dB for the output port corresponding to VSWRs of 1.62:1 and 1.67:1, respectively. Output powers at 1 dB, 2 dB, and 5 dB compression were measured and are reflected in the curves of Figure 6. Their minimum levels are at 15.5 dBm, 16.5 dBm, and 18.2 dBm respectively. At compression levels of up to 5 dB and an input signal of f = 2 GHz, the worst-case harmonic's output power does not exceed -15 dBc. Over the temperature range of -55°C to +95°, the small-signal gain varies fairly uniformly, as shown in Figure 7. The gain decreases a maximum of 2.8 dB and an average of about 2 dB across the band from +25°C to +95°C; as the temperature drops from +25°C to -55°C, the gain increases

a maximum of 2.0 dB and an average of 1.5 dB. A maximum gain variation of ΔG = 4.4 dB was measured over the entire temperature range. The maximum noise figure increased to NF = 8.1 dB at the elevated temperature of 95°C.

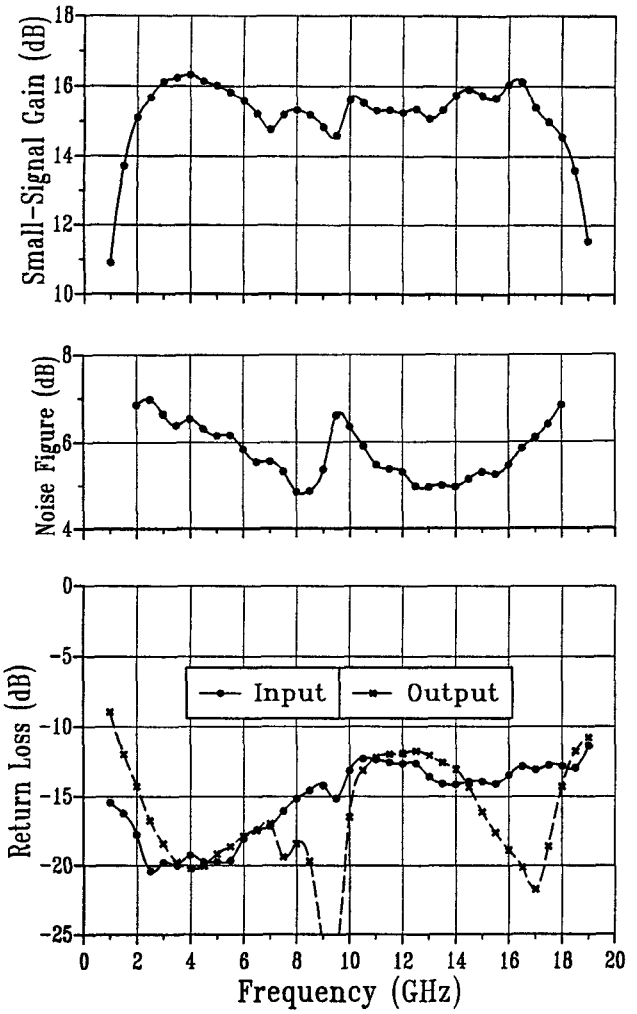

Figure 5 Gain, Noise Figure and Return Loss of the Experimental Amplifier

IV. SUMMARY

A two-tier monolithic matrix amplifier has been developed and tested. The unit's gain of G = 15.5 ± 0.9 dB at a maximum noise figure of NF = 7 dB and a minimum output power of $P_{1\,dB}$ = 15.5 dBm across the 2-18 GHz frequency band makes this single-stage module a very competitive device.

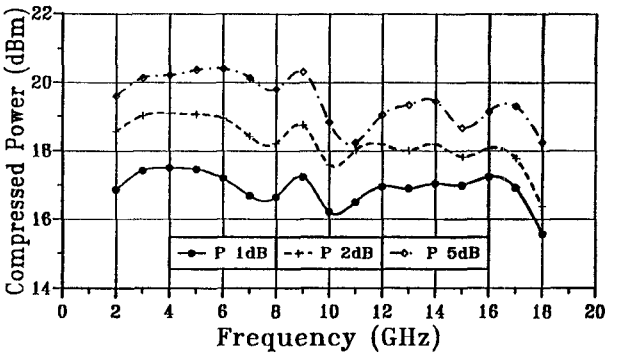

Figure 6 Compressed Output Powers of the Experimental Amplifier

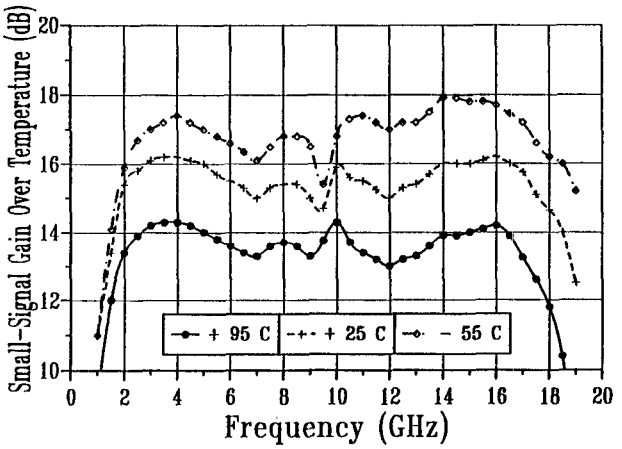

Figure 7 Gain Performance versus Temperature Curves

ACKNOWLEDGEMENTS

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